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Utilization of DVTS for Power Dissipation in Submicron Fabrication

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Abstract

Power dissipation is one of the critical design factors in microelectronics industry which opens lot of space for advance development in deep sub micron fabrication techniques for the devices. Low power design reduces cooling cost and increases reliability, especially for high density systems. Moreover, it reduces the weight and size of portable devices. In order to achieve the aim, static and dynamic component plays the main role in power dissipation of CMOS circuits. With the advent of new generations, power consumption of modern digital integrated circuits becomes a serious issue which is increasing continuously. To overcome this problem, a new idea has been proposed which reduces the consumption of power directly by controlling the supply voltage and body biasing, dynamically, and this can be done by DVTS scheme. Hence, Dynamic Voltage and Threshold scaling scheme preserves the leakage power during the active mode of the circuit.

Keywords: Dynamic Voltage and Threshold Scaling (DVTS), Low Power Design

Introduction

Area, performance, cost and reliability are the main concern for any VLSI designer. Low power design technique is more beneficial as power considerations are one of the important concern during the fabrication processes. Perhaps the primary driving factor has been the remarkable success and growth of the class of personal computing devices like portable desktops, audio & video based multimedia products and wireless communications systems which demand high speed computation and complex functionality with low power consumption. Minimizing power consumption in VLSI designs is the most important and desirable operation to be performed. We discussed on the various techniques for reducing the power consumption.

Power Dissipation Rootages

CMOS is the widely used technology for manufacturing digital & analog ICs. There are three major sources of power dissipation in a CMOS circuit:

$$P = P_{Switching} + P_{Short\text{-}Circuit} + P_{Leakage}$$

P Switching, known as *Switching Power*, is due to discharging and charging capacitors driven by the circuit. P Short-

Circuit is known as *Short-Circuit Power*, generated by the short circuit currents that occur when pairs of PMOS/NMOS transistors are conducting concurrently [9]. P Leakage is known as *Leakage Power*, generated from substrate injection and sub-threshold effects.

Power Minimization Techniques

Voltage Scaling

Voltage scaling is perhaps the most effective method of saving power due to the square law dependency of digital circuit active power on the supply voltage [10]. Total power consumption for microelectronic devices can be represented by:

$$P_{tot} = C_{tot} V_{dd}^2 f + V_{dd} I_{off}$$

The first term in above equation represents "switching power" (dynamic), while the second term represents "static power" which happens due to the leakage in the design. For low power design V_{DD} scaling is preferable but it decreases the circuit speed since $V_{GS} - V_T$, is reduced. To deal with this, systems may utilize dynamic voltage scaling to permit the lowest V_{DD} essential to meet the circuit speed necessities while saving the energy used for the computation [11, 12]. V_{DD} scaling enhances the gate delays unless the threshold voltage of the transistors is also scaled down. Due to the minimization of the threshold voltage there is a considerable rise in the leakage current of the transistors. Hence, there is a clear trade-off among the active power and off-state leakage for a specified application, leading to methodical selection of V_{DD} and V_T for performing an assigned task [6].

Reducing the physical Capacitance

Three basic types of capacitance in digital circuits, which are –

i. Gate Capacitance,
ii. Diffusion Capacitance, and

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iii. Interconnect Capacitance.

All these three components are scaled down by the same factor, then the net power dissipation is scaled down as well [12]. Gate and Diffusion Capacitances are fixed during the cell design, whereas Inter-cell and Global Interconnect Capacitances can be controlled by the CAD tools performing the global routing. Physical capacitance mainly reduces by the transistor sizing [8].

Reducing the switching frequency

Switching frequency may be reduced on several levels in the design process beginning from circuit level to the architectural level [13]. Power dissipating minimize during the transition of number from '0' to '1'. There is several logic styles to design and some of these styles are: Static CMOS, CPL, MCML, and a variety of dynamic logic styles. Generally, most logic styles perform delay power tradeoffs, but not always in proportional amounts [10]. The best style is that which minimize power dissipation at constant throughput.

DVTS Technique

Dynamic voltage and threshold scaling (DVTS) manages both dynamic and leakage powers by adjusting supply voltage (V_{DD}) and body bias voltage (V_{BB}). Total power of any digital circuit at desired performance level can be optimized by DVTS and this technique has been successfully proven on Si for low power & high speed applications. DVTS offers considerable power savings compared to DVS when leakage power is a large fraction of total power [1]. The power savings increase with increasing logic depth. The moderate performance of Application-Specific Integrated Circuit (ASIC) with long logic depth at low activity and/or high temperatures gain the most with DVTS.

DVTS Overview

Reduction of active leakage power is possible by dynamic V_{TH} Scaling (DVTS). Adaptive change in V_{TH} to a higher value thru V_{BB} when sagging during computation occurs. This will communicate an adequate amount of essential throughput for the current workload.

Hardware of DVTS contains a feedback loop which has voltage controlled oscillator (VCO), & charges pumps. For a certain workload the clock frequency of the system is determined by the operating system in run-time. The DVTS hardware reaches the best possible V_{TH} for the given clock frequency by animatedly adjusting the V_{BB}.

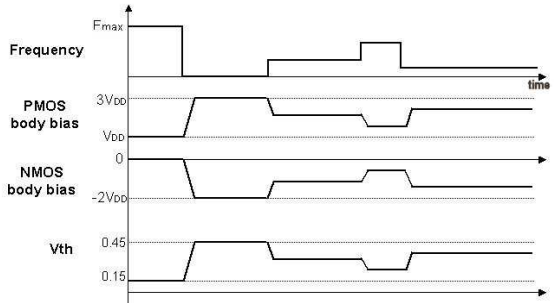

Fig.1 Dynamic V_{TH} scaling by adaptively changing the body bias
(Chris H. Kim et.al, Prude University, West Lafayette, IN 47907, USA [1])

Fig.1 shows how the DVTS system adaptively reins the body bias to change the V_{TH}. When the workload is less than the maximum for a given time period, the operating system will propose a lower clock frequency to the hardware [1]. For raising V_{TH} and reducing power dissipation, DVTS hardware will increase the PMOS body bias and decrease the NMOS body bias. To save the stand by leakage power, V_{TH} can be increased as much as the upper limit of V_{BB} when there is no workload at all. For reducing the total power, clock frequency will proportionally reduce. Scaling the supply voltage and reducing the clock rate together with the frequency saves power significantly [2].

Modules of DVTS System

V_{DD} Controller

V_{DD} will be scaled according to power consumption and time delay.

V_{BS} CONTROLLER

V_{BS} is the voltage between source and substrate where V_{BS} will affect threshold voltage. In DVTS approach both V_{DD} and V_{BS} will be scaled to decrease total power consumption [2].

Advantages of DVTS Over DVS

Further we here demonstrate how this scheme DVTS employed better result as compared to DVS scheme in terms of various parameters and become advantageous. Below some advantages are discussed.

Minimum Power Transition Loss

During charging/discharging cycle, under the DVS scheme V_{DD} ground capacitance is the power overhead. Even though there is no computation during this cycle and transition energy is consumed. For every low-to-high and high-to-low transition of supply voltage, current is evoked from power supply. Whereas, in DVTS the supply voltage is fixed to which less transition energy loss occurs during charging and discharging process [5].

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No Requirement of Voltage Converters

DVTS systems employ the same supply voltage all through the chip, no voltage level converters are essential. Although the conventional level converter keeps static power consumption. The dynamic power consumption is hefty as much as necessary to cancel out the power savings gained from supply voltage scaling [7].

Voltage Boosting Facility Via Simple Hardware

Buck converters are used in DVS systems which requires external inductors and having more power consumptions, but not in DVTS system. DVTS system uses charge pumps to generate the body bias voltages which provide effortless solution for boosting the voltages.

Cross Talk Reduction

Noise immunity is improved in DVTS scheme by increasing $V_{TH,}$ specifically for all noise susceptible circuits such as flip-flops, registers etc. Here, signal integration becomes more important issue for all micron family devices so that cross talk reduced between similar energy levels.

Conclusion

The paper emphasise basically on DVTS scheme whose outcome explains as to how the overall reduction in switching frequency achieved along with the physical capacitance and voltage scaling proficiencies for power minimization of all sub-micron family devices over to the DVS scheme. The aim of work is to resolve the problem of power dissipation, which is an important concern in deep sub micron fabrication of devices. Hence, we investigated the same through various other merits of DVTS in comparison with DVS scheme. Thus, by considering these factors, we can use this technology for designing and characterising new cell library for ultra low power cells in deep sub-micron region and which can also help at RF level works. Now, it can be extrapolated that for huge leakage currents, DVTS is more beneficial over DVS.

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